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TRACKED 3X OVERSAMPLING RECEIVER

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CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of co-pending U.S. Patent Application entitled "Frequency Comparator With Hysteresis Between Locked And Unlocked Conditions", serial number 10/356,695 (attorney docket no. 59472-8086.US01), filed on January 30, 2003, and is incorporated herein by reference, which is a continuation of U.S. Patent Application entitled "0.6-2.5 Gbaud CMOS Tracked 3X Oversampling Transceiver With Dead Zone-Phase Detection for Robust Clock Data Recovery", serial number 10/305,254 (attorney docket no. 59472-8079.US01) filed on November 25,2002 and is incorporated by reference, which claims the benefits of U.S. Provisional Patent Application entitled "0.6-2.5 Gbaud CMOS Tracked 3X Oversampling Transceiver With Dead Zone-Phase Detection for Robust Clock Data Recovery", serial number 60/333,439 (attorney docket no. 59472-8079.US00), filed on November 26, 2001, and is incorporated herein by reference. U.S. Patent Application entitled "Frequency Comparator With Hysteresis Between Locked And Unlocked Conditions", serial number 10/356,695 (attorney docket no. 59472-8086.US01), filed on January 30, 2003 (which the present application is a continuation of) is also a Continuation-in-Part and claims the benefits of U.S. Patent Application entitled "Implementing an Oversampling Transceiver with Dead-Zone Phase Detection", serial number 09/948,123 (attorney docket no. 59472-8055.US01) filed on September 5, 2001, which is also incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention relates to the field of data communications. In particular the present invention discloses methods and circuits for robust data recovery on a high-speed serial data link.

BACKGROUND OF THE INVENTION

[0003] As serial links are required to operate at higher frequencies and over longer distances, more sophisticated mechanisms have been adopted to recover data from more severely degraded signals. However, conventional serial transceiver systems have shortcomings. For example, a conventional transmitter uses a conventional current mode-driver whose speed is limited to 0.43/RC due to a passive pull-up resistor. Furthermore, if a Delay-Locked Loop (DLL) is used in a transmitter, special consideration must be made in designing a wide-range multi-phase DLL due to a so-called stuck problem.

[0004] In a conventional receiver system that uses using oversampling, the receiver Phase-Locked Loop (PLL) is locked to a reference clock rather than to the transmitted signal. In a tracked two-times (2X) oversampling receiver, two samples are made per bit, one for the data sampling and the other for edge tracking. Prior art Two-times (2X) sampling pulses are illustrated in **fig. 1B**. The sampled bits are examined to determine whether to move the sampling clock phase earlier (UP) or later (DOWN). In a prior art receiver that uses two-times (2X) sampling, the decision is binary: either UP or DOWN. **Figure 1C** illustrates the prior art number of UP and DOWN pulses issues **90** by a phase adjustment circuitry from the jitter of **Figures 1A** and **1B**.

[0005] When a two-times (2X) sampling system has reached a locked state, the number of UP pulses is equal to the number of DOWN pulses. Thus, the phase adjustment circuitry tends to oscillate when it is in a locked steady state. Furthermore, in such a 2X sampling system, the clock edge for data sampling could be quite off from the optimum center point as illustrated in **fig. 1A**. This misplacement of the sampling clock is due to the asymmetric nature of severe jitter as illustrated by the histogram in **fig. 1B**, and is not desirable.

[0006] Also, a conventional tracked three-times (3X) oversampling phase detector raises several design problems due to long pumping pulses persisting for one Voltage Controlled Oscillator (VCO) cycle time. (See Inyeol Lee, et al. "A 622Mb/s CMOS Clock Recovery PLL with Time-Interleaved Phase Detector Array," ISSCC Digest of Technical papers, pp. 198-199, Feb. 1996.)

[0007] For better jitter performance, the Phase-Locked Loop should have a structure that is more immune to power-supply noise. The Phase-Locked Loop should also contain a smaller number of possible noise sources.

[0008] Conventional Voltage Controlled Oscillators (VCOs) that use replica bias circuits are known to produce most of their jitter due to the noise in the bias voltage from the replica circuit. (See Ian A. Young, et al., "A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessors," IEEE JSSC, vol. 27, pp. 1599-1607, Nov. 1992.) Due to these and other shortcomings of prior art transceiver systems, there is a need for an improved transceiver that provides robust clock and data recovery.

SUMMARY OF THE INVENTION

[0009] The present invention introduces a transceiver that performs three-times (3X) oversampling and dead zone detection in order to stabilize the voltage controlled oscillator (VCO) when the proper sampling frequency has been reached.

[0010] A method of receiving data, in accordance with an embodiment of the present invention, includes the acts of generating a data sampling clock signal and comparing a received clock signal to the data sampling clock signal. The data sampling clock signalis used to sample a data signal into sampled data representing a first zone, a second zone, and a third zone of the data signal. It is then determined which zone of the sampled data has a transition of the data signal and indicating a direction of change for the data sampling clock signal if the first zone or the third zone has the transition.

[0011] A receiver apparatus, in accordance with another embodiment of the present invention, includes a phase locked loop circuit including a voltage controlled oscillator used to generate a data sampling clock signal. A data sampler is used to receive the data sampling clock signal, to sample a data signal using the data sampling clock signal, wherein the frequency of the data sampling clock signal is three times greater than the data signal frequency, and to output sampled data representing a first zone, a second zone, and a third zone of the data signal. A phase detector is used to examine the sampled data, to determine which zone of the sampled data has a transition of the data signal, and to output a phase detector signal indicating a direction of change for the data sampling clock signal if the first zone or the third zone has the transition. Also included is a frequency comparator that compares the frequencies of the data sampling clock produced by the voltage controlled oscillator and a reference clock signal.

[0012] A method of controlling a receiver to receive data, in accordance with a final embodiment of the present invention, includes the steps of generating a data sampling clock signal and sampling a data signal using the data sampling clock signal, wherein the frequency of the data sampling clock signal is three times greater than the data signal frequency, and outputting sampled data representing a first zone, a second zone, and a third zone of the data

signal. The sampled data is detected to determine which zone of the sampled data has a transition of the data signal, and to output a phase detector signal indicating a direction of change for the data sampling clock signal if the first zone or the third zone has the transition. The frequencies of the data sampling clock and a reference clock signal are then compared.

[0013] The transceiver of the present invention incorporates a voltage-mode driver, on-chip mid-supply terminator, an analog multi-phase delay-locked loop (DLL), a tracked 3X oversampling technique with dead-zone phase detection, and a phase-locked loop (PLL) with folded starved-inverter delay cells. The implemented transceiver was proven to transmit and recover data at 2.5GBaud over a 10 meter 150Ω Single-Twisted-Pair (STP) cable and at 1.25GBaud over a 25 meter Single-Twisted-Pair (STP) cable with a Bit Error Rate (BER) of less than 10^{-13}.

[0014] These and other advantages of the present invention will become apparent to those skilled in the art upon a reading of the following detailed descriptions and a study of the various figures

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Figure 1A illustrates a prior art eye diagram for a received signal.

[0016] Figure 1B illustrates a prior art asymmetric jitter distribution histogram for the signal of fig. 1A and sampling clocks in a two-times (2X) oversampling receiver system.

[0017] Figure 1C illustrates the prior art UP and DOWN pulses for a Voltage Controlled Oscillator from the signal of fig. 1A.

[0018] Figure 2 illustrates a simplified block diagram of a serial link transceiver, in accordance with the present invention.

[0019] Figure 3 illustrates a more detailed block diagram of the transceiver device, in accordance with the present invention.

[0020] Figure 4 illustrates a more detailed block diagram of the frequency comparator.

[0021] Figures 5A and 5B illustrates a schematic diagram of a DLL used in the present invention.

[0022] Figure 5C illustrates a schematic diagram of a delay cell element used in the DLL of fig. 3A.

[0023] Figure 5D illustrates a schematic diagram of a current steering phase detectors used in the DLL of fig. 5B.

[0024] Figure 5E illustrates a timing diagram of the clock waveforms when the DLL of fig. 4A is in a locked state.

[0025] Figure 6A illustrates an eye diagram for a received signal.

[0026] Figure 6B illustrates an asymmetric jitter distribution histogram for the signal of fig. 5A and sampling clocks in a three-times (3X) oversampling receiver system.

[0027] Figure 6C illustrates the UP and DOWN pulses for a Voltage Controlled Oscillator from the signal of fig. 6A.

[0028] Figures 7A to 7E illustrate timing diagrams that cause various phase adjustments as set forth in Table 1.

[0029] Figure 8 is a schematic diagram of a folded starved inverter with a supply regulator used in the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0030] A method and apparatus for implementing an oversampling transceiver with dead-zone phase detection is disclosed. In the following description, for purposes of explanation, specific nomenclature is set forth to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that these specific details are not required in order to practice the present invention. For example, certain teachings of the present invention have been described with reference to a phase-locked loop circuit in a data communication transceiver device. However, the signal phase comparison and locking techniques of the present invention can easily be applied to other types of phase-locked loop applications or in other applications that require a phase comparison.

[0031] TRANSCIEVER ARCHITECTURE OVERVIEW

[0032] **Figure 2** illustrates a simplified block diagram of a serial link transceiver **100**, in accordance with the present invention. Included is a 75 ohm cable-in **10**, a receiver **100**, a multi-phase DLL **130**, a transmitter **180** and a 75 ohm cable-out **20**. Also included is a comma detector **100**.

[0033] **Figure 3** illustrates a more detailed block diagram of the transceiver device **100**, in accordance with the present invention. The main components of the transceiver device **100** are the receiver **110** and the transmitter **180**.

[0034] TRANSMITTER OVERVIEW

[0035] The transmitter **180** of the transceiver device **100** illustrated in **Figure 3** is composed of a wide operating range multi-phase Delay-Locked Loop (DLL) **181**, a serializer **185**, and a voltage-mode driver **187**. The voltage-mode driver **187** exhibits both active pull-up and active pull-down, and maintains its speed regardless of the cable impedance. Furthermore, the voltage-mode driver **187** can be AC coupled to a cable without any additional resistors.

[0036] A Delay-Locked Loop (DLL) **181** rather than a Phase-Locked Loop (PLL) is used in the transmitter **180** of the present invention to avoid jitter peaking which causes the jitter

components near the bandwidth to be amplified rather than being suppressed when the receiver PLL has the similar bandwidth as the transmitter's. Since the Delay-Locked Loop (DLL) **181** has different frequency characteristics, such jitter peaking does not occur. The only concern is to build a Delay-Locked Loop (DLL) **181** with a wide frequency range, which will be explained below.

[0037] RECEIVER OVERVIEW

[0038] The receiver **110** of the transceiver device **100** illustrated in **Fig. 3** is composed of on-chip termination resistor **111**, oversamplers **120**, a multi-phase Phase-Locked Loop (PLL) **130**, a dead-zone phase detector **150**, and a frequency comparator **160**. The receiver Phase-Locked Loop (PLL) **130** tracks the transmitter clock frequency. Thus, clock recovery is accomplished in the Phase-Locked Loop **130**.

[0039] The Voltage Controlled Oscillator **131** of the Phase-Locked Loop **130** produces a clock signal to have the oversamplers **120** sample the incoming signal at three-times (3X) the bit frequency.

[0040] While the digital Phase-Locked Loop **130** based 3X oversampling architecture has an inherent static sampling phase error up to 1/6 bit time and shows abrupt phase jump in the recovered clock due to phase quantization, the architecture of the present invention reduces such sampling error and avoids the phase jump in the presence of excessive amount of jitter in the data stream. Delay cells with a folded starved inverter configuration are used in the Voltage Controlled Oscillator (VCO) to exhibit less jitter and more tolerance against supply noise.

[0041] The dead-zone phase detector **150**, of which detailed operation will be explained later, examines the sampled data and determines the direction of change for the Voltage Controlled Oscillator (VCO) **131** frequency. The dead-zone phase detector **150** is activated only after frequency lock is obtained when the external reference clock frequency and the Voltage Controlled Oscillator **131** frequency are within 200ppm of each other.

[0042] The frequency comparator **160** is designed to have a hysteresis between its lock and unlock states in order to interact with the Phase-Locked Loop **130** in a compatible manner and to lock more robustly to the reference clock. Specifically, the frequency comparator **160** is deactivated when the external reference clock frequency and the Voltage Controlled Oscillator **131** frequency are within 200ppm of each other, but the frequency comparator **160** is only reactivated when the external reference clock frequency and the Voltage Controlled Oscillator **131** are greater than 1000ppm of each other.

[0043] **Figure 4** illustrates a more detailed block diagram of the frequency comparator **160**. As previously stated, the frequency comparator has hysteresis between the lock and unlock conditions. A 16-bit binary counter **162**is updated at VCO-CLK cycle. A 14 bit divider **164** divides the Ref-CLK. Latch U2 samples the binary counter value at the divided Ref-CLK ridges. However, the Ref-CLK and VCO-CLK domains are asynchronous with each other. As a result, there is a possibility that the latch U2 will fall ino meta-stability when transmitted value changes on the sampling edge of the Ref-CLK. Since some bits have been changed while others have not at the sampling time, the sampled value can possibly be very different from the original value. To prevent this meta-stability problem, a binary-to-gray code converter **166** is inserted before the latching stage to allow only one bit to be inverted whenever the counter value is updated.

[0044] OTHER TRANSCEIVER CIRCUITS

[0045] Referring back to fig. 3, a comma detector **192** in the transceiver device **100** monitors the incoming data stream **30** to search for a K28.5 pattern in IBM 8B/10B coding for byte alignment. For ease of testing at the full speed, the transceiver device **100** includes an integrated Built-In Self Test (BIST) circuit **199**. The Build-In Self Test (BIST) circuit includes Pseudo Random Bit Stream (PRBS) generation **40**, verification (not shown), and Bit Error Rate (BER) counting logic (not shown).

[0046] DLL DESIGN

[0047] Figures 5A-D illustrate the structure and operation of one embodiment of a Delay-Locked Loop (DLL) **181** circuit for the transceiver of **fig. 2**. A new DLL architecture is shown to widen its range further in an architecture level.

[0048] Figure 4A illustrates a Voltage-Controlled Delay Line (VCDL) circuit **201** that consists of 10 delay cell elements (**210, 211, ... 219**) and generates the same number of clock outputs. **Figure 4B** illustrates one possible embodiment of the internal structure of each delay cell element (**210, 211, ... 219**).

[0049] For the main phase detector (PD_1) in **fig. 5B** to work around the stuck and harmonic-lock problems, the initiai T_{VCDL} value should satisfy the following inequality, as shown in equation I:

[0050] $$0.5 \times T_{CLK} < T_{VCDL} < 1.5 \times T_{CLK} \qquad \text{(EQUATION I)}$$

where T_{CLK} is the period of the reference clock.

[0051] However, the range of T_{VCDL} is generally wider than the above restraint and the initial value of T_{VCDL} is not known at the start-up time. To put the initial T_{VCDL} within the range in the preceeding inequality (equation I), two Current Steering Phase Detectors (CSPDs) **50** and **60** are used. Specifically, **fig. 5B** illustrates $CSPD_1$ **50** and $CSPD_2$ **60**. Since the upper to lower current ratio is tuned to 3:1 as illustrated in **figure 5C**, Ref-CLK, CLK0, and CLK1 maintain the delay relationship illustrated in the timing diagram of **figure 5E**. It can be summarized in the following inequalities, as shown in equation II:

[0052] $$T_{DC} < 1/8 \times T_{CLK} \text{ and } 2 \times T_{DC} > 1/8 \times T_{CLK} \qquad \text{(Equation II)}$$

[0053] Or equivalently in terms of T_{VCDL}, as shown in equation III:

[0054] $$5/8 \times T_{CLK} < T_{VCDL} < 5/4 \times T_{CLK} \text{ (therefore } T_{DC} = 1/10 \times T_{VCDL}) \qquad \text{(Equation III)}$$

where T_{DC} is Ref-CLK to CLK0 delay and 2x T_{DC} is Ref-CLK to CLK1 delay.

[0055] In such a locked state, the Q_1 output from $CSPD_1$ is '0' and the Q_2 output from $CSPD_2$ is '1' as illustrated in the timing diagram **fig. 5E**. Thus, referring back to **fig. 5B**, "gup" and "gdown" become '0' and "glock" become '1'. Then, CP_0 is disabled and PD_1 is activated. Since inequality (equation III) satisfies inequality (equation I) in the control hand-over, the transition is smooth and PD_1 removes the residual phase error between Ref-CLK and CLK9 without losing the lock.

[0056] PD_2 (fine phase detector) is also activated and performs cell-level duty-cycle correction. In this manner, multi-phase clocks are made equally spaced with a 50% duty-cycle. The condition for correct Current Steering Phase Detector (CSPD) operation is as follows:

[0057] $$T_{DC.max} (= 1/10 \times T_{VCDL.max}) < 7/8 \times T_{CLK} \qquad \text{(Equation IV)}$$

[0058] This inequality determines the lower bound of the Delay-Locked Loop operating range as follows:

[0059] $$4/35 \times T_{VCDL.max} < T_{CLK} \leq T_{VCDL.max} \qquad \text{(Equation V)}$$

[0060] Thus, the theoretical operating frequency range of the circuit is 8.75:1, which is wide enough for many applications.

[0061] DEAD ZONE PHASE DETECTION

[0062] In high bandwidth communication systems over a long distance, the receiver should be able to operate in the worst case when the total jitter of the incoming data signals is less than or equal to about 40% of a bit time. The total jitter is the sum of deterministic and random jitter. The deterministic jitter includes the effect of systematic variation of bit times

and Inter-Symbol Interference (ISI). The deterministic jitter generally provides the major portion of the total jitter in a long copper cable.

[0063] When a receiver finally receives a signal that was transmitted over a long cable, the received signal is severely degraded. One specific type of degradation is jitter, a time-based distortion of the received signal. Jitter causes the signal transition time to vary. For example, **Figures 1A** and **6A** illustrate an eye diagram of a signal **60** and **62** that has been degraded by jitter. Note that there is no clean signal transition edge **70** or **74** in **figs. 1A** and **6A**.

[0064] **Figures 1B** and **6B** illustrate a histogram of the jitter distribution **80** and **82** of the signals **60** and **62** in **figs. 1A** and **6A**, respectively. Due to systematic variation of bit times and various other reasons, the jitter histograms are often found to be asymmetric and have a longer tail **80a** and **82b** in one direction.

[0065] The purpose of the phase detection in a receiver circuit is to have the sampling clock located at the middle of the "data eye" in the eye diagram **60** and **62** of **figs. 1A** and **6A**. This will minimize the bit error rate when recovering data from a severely degraded signal.

[0066] 3X OVERSAMPLING WITH DEAD ZONE DETECTION

[0067] The system of the present invention prevents such an oscillation at the locked state and optimizes the placement of the data-sampling clock. Specifically, the present invention introduces a tracked three-times (3X) oversampling with "dead-zone" detection. In the system of the present invention, only the extreme tail portions of the jitter histogram activate the phase adjustment circuitry. The edges located in the "dead-zone" (the middle portion of one-third of the bit time) are ignored for phase comparison. Thus, the phase adjustment circuit is active less often as illustrated in the UP and DOWN pulse diagram of **fig. 6C**.

[0068] The dead-zone detection circuit may operate by comparing the bit values of two consecutive data samples and the two edge detection samples that occur between the two consecutive data samples. The following **Table I** provides a truth table of how the data edge bits. **Table I** can be viewed with reference to **Figures 7A** to **7E**.

[0069] TABLE I

Data N	Edge 1	Edge 2	Data N+1	Phase Adjustment	Figure
0	0	0	0	No Change (No Transition)	
0	0	0	1	DOWN	**Figure 7C**
0	0	1	0	No Change (No Transition)	
0	0	1	1	No Change (Dead Zone)	
0	1	0	0	No Change (No Transition)	
0	1	0	1	Should not occur.	
0	1	1	0	No Change (No Transition)	
0	1	1	1	UP	**Figure 7E**
1	0	0	0	UP	**Figure 7D**
1	0	0	1	No Change (No Transition)	
1	0	1	0	Should not occur.	
1	0	1	1	No Change (No Transition)	
1	1	0	0	No Change (Dead Zone)	**Figure 7A**
1	1	0	1	No Change (No Transition)	
1	1	1	0	DOWN	**Figure 7B**
1	1	1	1	No Change (No Transition)	

[0067] Since the data sampling points are driven toward the center of the data eye only with the worst-case edges, the operation of the 3X oversampling system with dead-zone detection is more robust in the presence of excessive jitter, where bit errors are more likely. Furthermore, the system of the present invention does better job of keeping the data sampling clock at the center of the data eye as illustrated by **fig. 6A**.

[0068] Although the width of the dead-zone can be varied, simulation has proved that the dead-zone of one-third of a bit time offers quite adequate performance. Furthermore, a one-third of a bit time dead zone can be easily implemented with a 3X oversampling clock. Interestingly, the clock recovered from the data stream is expected to contain more jitter when the incoming serial data signal is clean. In such a case, the clock edges drift by up to one third of a bit time. However, the bit error rate is very low in such circumstances.

[0069] The design of the present invention reduces the pulse width to one bit time, thereby avoiding using an extremely small pumping current. Furthermore, due to the wide tolerance

of the phase detection mechanism, the design of the present invention exhibits a wide frequency range operation without the pumping current control under PVT variations of PLL components.

[0070] PLL Design

[0071] Figure 8 illustrates a schematic diagram of a folded starved inverter for use in the Voltage Controlled Oscillator (VCO) of one embodiment of the present invention. A cross-coupled PMOS pair is included to sharpen the transition edges of the output waveform regardless of the delay time. The inverters, G_1 and G_2, give more linearity to the VCO gain and its positive supply-sensitivity compensates the negative supply-sensitivity of the starved cell.

[0072] To reduce the effect of a power supply fluctuation further, a supply regulator **620** is added. Resistors and capacitors filter out the high frequency components of the 3.3V supply and provide a clean voltage to the gate of a NMOS source follower. Simulation results show that a VCO implemented according to **Figure 8** has about 10 times smaller supply sensitivity (0.23ps/mV) and substrate sensitivity (0.26ps/mV) and 15dB less phase noise than a typical VCO.

[0073] EXPERIMENTAL RESULTS

[0074] A prototype chip has been fabricated with a 0.25μm CMOS process. The DLL operating range is 30MHz to 250 MHz with less than 2% timing error among clock phases. Board level testing shows that the transceiver operates at 2.5GBaud over a 10-meter 150Ω Single-Twisted-Pair (STP) cable and at 1.25GBaud over a 25 meter Single-Twisted-Pair (STP) cable with 25% eye opening with no error detected for more than 3 hours (A Bit Error Rate (BER) of less than 10^{-13}).

[0075] Due to the operation of the dead-zone phase detection circuit **150** of the present invention, the recovered clock jitter is actually reduced as the jitter increases in the serial data signals. In an extreme case at 1.25GBaud, recovered clock jitter is reduced down to 28ps, RMS when the signal jitter is 111ps, RMS. On the other hand, when there is little jitter in the

serial data signal, relatively large jitter of 40ps, RMS is observed at the receiver but without any bit error.

[0076] When the Phase-Locked Loop **130** of the receiver **110** is locked to the reference clock at 187MHz, the measured jitter is 5.5ps, RMS and 35ps, peak-to-peak. The following **Table II** summarizes the measured performance of the transceiver circuit as implemented in 0.25 μm CMOS semiconductor process technology.

[0077] TABLE II

Semiconductor Process		0.25 μm N-well 4-metal CMOS process
Supply voltage		2.5V (core), 3.3V (I/O)
DLL frequency range		30 – 250 MHz
Data rate range		0.6 – 2.6 GBaud
Area	Total	4.9 mm^2
	DLL	0.1 mm^2
	PLL	0.36 mm^2
Power dissipation	Total	57.5 (mW/GBaud) x Data rate + 125.5 (mW) (197mW @ 1.25GBaud, 269mW @ 2.5GBaud
	DLL	16.8mW @ 125GBaud
	PLL	29.4mW @ 1.25GBaud (6.6mW for VCO only)
Accumulated Jitter	Tx data	7.3 ps RMS / 46 ps peak-to-peak
(with link activated)	DLL	6.0 ps RMS / 40 ps peak-to-peak
(@ 1.87 GBaud)	PL	5.5 ps RMS / 35 ps peak-to-peak
Bit Error Rate (BER)		$<10^{-13}$ with a 10m 150Ω Single-Twisted-Pair (STP) cable @ 2.5GBaud $<10^{-13}$ with a 25m 150Ω Single-Twisted-Pair (STP) cable @ 12.5GBaud

[0077] The foregoing has described a method and apparatus for implementing an oversampling transceiver with dead-zone phase detection. It is contemplated that changes and modifications may be made by one of ordinary skill in the art, to the materials and arrangements of elements of the present invention without departing from the scope of the invention.